REMARKS

Upon entry of the present Amendment, claims 1-20 are all the claims pending in the application. Claims 1, 4, 11, and 15 are amended, and new claims 19 and 20 are added. No new matter is presented.

Dealing with preliminary matters first, Applicant notes that the Examiner has not indicated acceptance of the drawings filed on March 4, 2004. Thus, the Examiner is kindly requested to indicate acceptance of these drawings in the next action.

In addition, Applicant notes that the Examiner has not acknowledged Applicant's claim for foreign priority based on JP 2002-216607. Accordingly, the Examiner is requested to acknowledge the claim for foreign priority and to indicate acceptance of the certified copy of the priority document in the next action.

To summarize the Office Action, claims 1-3 and 8-14 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Omoda et al. (U.S. Patent No. 4,680,730, hereinafter "Omoda") in view of Suzuki (U.S. Patent No. 6,240,524), further in view of Nishi (U.S. Patent No. 5,241,633), and claims 4-5 and 15-16 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Omoda in view of Suzuki and Nishi, further in view of Lee et al. (U.S. Patent No. 6,629,271, hereinafter "Lee"). Further, the Examiner objected to claims 6-7 and 17-18 as being dependent upon a rejected base claim, but indicated that these claims would be allowable if rewritten in independent form including all the limitations of their base claims and any intervening claims. The outstanding rejections and objections are addressed below.

Claim Rejections - 35 USC § 103

Omoda in view of Suzuki and Nishi

As noted above, claims 1-3 and 8-14 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Omoda in view of Suzuki, and further in view of Nishi. This ground of rejection is traversed.

With respect to independent claim 1, Applicant submits that claim 1 defines a novel vector information processing apparatus presenting new features. For instance, the apparatus defined by claim 1 comprises, *inter alia*, a CPU comprising a plurality of asynchronously operating units, a main memory for storing data; and a main memory controller for controlling the writing of data in said main memory. Further, the main memory controller includes a vector scatter (VSC) address buffer that holds a storage address in said main memory for each element designated by a vector scatter instruction. In addition, the main memory controller inhibits the outputting of a writing permission signal that permits writing to the main memory which is generated according to a writing request that requests writing of an element having a smaller element number than at least one other element designated by the vector scatter instruction if the writing request instructs storage of the element at an identical storage address as the at least one other element and the writing request has not been processed in accordance with a sequence of element numbers defined by the vector scatter instruction. Also, claim 1 recites the features of writing requests for writing the element and the at least one other element to the storage address in said main memory are issued respectively from the asynchronously operating units of the CPU according to the vector scatter instruction.

Notwithstanding the Examiner's rejection, Applicant submits that the combination of Omoda in view of Suzuki and Nishi fails to teach or suggest all the features of claim 1. For example, none of Omoda, Suzuki or Nishi suggests controlling the writing of data to memory in accordance with a vector scatter instruction, as claimed. In this regard, Applicant notes that the Examiner contends that Omoda discloses a memory controller having a vector scatter address buffer for holding a storage address for each element designated by a vector scatter instruction. *See* Office Action at pages 2-3. However, Omoda merely teaches a storage control apparatus in which only vector elements that are selected according to mask information are stored in permanent memory locations of a desired vector register. *See* Omoda at col. 1, lines 56-63. As taught by Omoda, each vector element of a vector is compared with a constant data "0.0" and a bit mask is generated which indicates locations where the vector elements are determined to be equal to "0.0". *See* Omoda at col. 1, lines 17-30 and col. 3, lines 35-44. As a result of the bit mask information indicating the elements which have a zero value, only the elements which have a value other than zero are stored in corresponding memory locations, and write operations are not executed for the other memory locations. *See* Omoda at col. 3, lines 16-24.

The selective writing of vector elements based on a mask value does not teach or suggest a vector scatter instruction, as claimed. For instance, a vector scatter instruction is well known in the art as a process in which vector elements are successively written into memory in the sequence of element numbers. *See, e.g.*, Specification at page 5. By contrast, Omoda teaches that only certain elements of a vector are written into memory. In other words, only the vector elements that which are not determined to have a "0.0" values are written to memory. Thus, as

Omoda's selective writing of elements clearly teaches that certain elements of the vector will be skipped, Omoda cannot properly be relied upon to teach a vector scatter instruction, as claimed, and therefore further fails to suggest at least the feature of a writing request that requests writing of an element having a smaller element number than at least one other element designated by the vector scatter instruction, which has an identical storage address as said at least one other element.

Further, the teachings of Suzuki and Nishi fail to compensate for the deficiencies of Omoda. For example, the Examiner asserts that "Omoda does not describe the claim's detail of asynchronous operating units", and relies on Suzuki which is alleged to teach a processor with multiple functional units (referencing circuit blocks 90 and 92 and col. 11, lines 22-33). *See* Office Action at page 3. However, Suzuki merely teaches that "circuit blocks" of a semiconductor, such as the superscalar processor depicted in Figure 11, may be supplied with different clock signals to prevent clock skew which would occur if a single clock signal were distributed to the "whole of the chip." *See* Suzuki at col. 2, lines 54-65 and col. 11, lines 22-57. Thus, Suzuki suggests nothing about a vector scatter instruction, as claimed.

Moreover, Applicant notes that claim 1 additionally recites the feature of wherein writing requests for writing said element and said at least one other element to said storage address in said main memory are issued respectively from said asynchronously operating units of said CPU according to said vector scatter instruction. Suzuki further fails to suggest asynchronously operating units of a CPU respectively issuing writing requests for vector element according to a the vector scatter instruction. Indeed, Applicant notes that the elements relied upon in Suzuki as

"asynchronously operating units" are first circuit block 90 and second circuit block 91. *See* Office Action at page 3. The first circuit block 90 is described as including a program counter, an incrementer, an instruction cache, and a branch prediction unit. *See* Suzuki at col. 11, lines 25-27. Further, the second circuit block 91 is described as including a first instruction decoder, a second instruction decoder, a first register file, and a second register file. *See* Suzuki at col. 11, lines 27-29.

However, Suzuki does not suggest that the first circuit block 90 and the second circuit block 91 respectively issue writing requests. Rather, Suzuki merely teaches that different "blocks" of the processor may be supplied with a different clock to prevent clock skew. Thus, even if combined with Omoda, the teaching of Suzuki would fail to suggest writing requests issued respectively from asynchronously operating units as claimed, and the combination would additionally fail to teach writing requests according to a vector scatter instruction, for the reasons discussed above.

Further, the teaching of Nishi likewise fails to compensate for the deficiencies of the combined teaching of Omoda and Suzuki. In this regard, Applicant notes that the Examiner alleges that "Nishi describes a circuit to detect the address contention for requests to memory". *See* Office Action at pages 3-4. However, as shown below, even if the teaching of Nishi were combined with Omoda and Suzuki, the combined teaching would nonetheless fail to suggest all the features of claim 1.

For instance, Nishi teaches instruction sequence control to allow parallel or simultaneous execution of instructions in which two instructions are loaded for sequence determination.

Subsequently, Nishi teaches that the system checks for "passability of an instruction", which requires determination of whether either instruction is determined to read from or write into the other instruction, both instructions reference the same address, and if either instruction will contend with a currently executing instruction for the registers, arithmetic unit, or main memory. *See* Nishi at col. 2, lines 42 - col. 3, line 12 and col. 4, lines 48-58. However, Nishi does not suggest a vector scatter instruction, as claimed, but rather teaches determination of instruction passability with respect to vector load, vector add, vector multiplication and vector store instructions. *See* Nishi at col. 7, lines 38-50.

Indeed, column 10, line 65 - col. 11, line 20, which the Examiner relies upon in the grounds of rejection, merely teaches the determination of whether a second vector store instruction referencing the main memory overlaps a first vector store instruction. Thus, Nishi does not teach contention of elements within a vector, but rather teaches contention with respect to writing elements of different vectors. Therefore, Nishi cannot properly be relied upon to teach the feature of inhibiting the outputting of a writing permission signal that permits writing to the main memory which is generated according to a writing request that requests writing of an element having a smaller element number than at least one other element designated by the vector scatter instruction if the writing request instructs storage of the element at an identical storage address as the at least one other element and the writing request has not been processed in accordance with a sequence of element numbers defined by the vector scatter instruction, which is clearly deficient in Omoda and Suzuki, as evidenced by the above discussion. Further, Applicant notes that Nishi fails to suggest instructions issued by asynchronously operating units,

as claimed, which has likewise demonstrated to be deficient in the combination of Omoda and Suzuki.

Therefore, even assuming *arguendo* that the Examiner asserted motivation to combine the teachings of Omoda, Suzuki and Nishi is proper, the combination would fail to suggest all the features of the vector information processing apparatus defined by claim 1. As a consequence, the Examiner has failed to establish *prima facie* obviousness with respect to the combination of features defined by claim 1. Reconsideration and withdrawal of the rejection are therefore requested.

Further, Applicant submits that the above arguments are equally applicable to independent claim 11, which defines a method for controlling a memory of a vector processing apparatus reciting similar features. Thus, claim 11 is believed to be allowable for similar reasons. With respect to dependent claims 2-10 and 12-20, Applicant submits that these claims are allowable at least by virtue of depending from claims 1 and 11, respectively. Allowance of these claims is therefore requested.

Omoda in view of Suzuki and Nishi, further in view of Lee

Without commenting substantively on the grounds of rejection, Applicant submits that claims 6-7 and 17-18 are allowable at least by virtue of depending from claims 1 and 11. Accordingly, reconsideration and withdrawal of this ground of rejection is requested

New claims

In order to provide additional claim coverage merited by the scope of the invention, Applicant is adding new claims 19 and 20, which depend from claims 1 and 11, respectively. As

noted above, these claims are believed to be allowable at least by virtue of depending from claims 1 and 11.

Further, Applicant notes that claims 19 and 20 require that writing requests for writing the element and the at least one other element to the storage address in the main memory are issued respectively from different asynchronously operating units of the CPU according to the vector scatter instruction. The combination of Omoda, Suzuki and Nishi fails to suggest this feature. As discussed above, the Examiner alleges that Suzuki teaches asynchronous operating units. However, as clearly evidenced by the foregoing, the teaching of Suzuki does not suggest different asynchronous operating unit issuing writing requests according to a vector scatter instruction. Further, at least for the reasons discussed above, the teachings of Omoda and Nishi fail to compensate for this deficiency.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned attorney at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

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